# EE 330 Laboratory 5
# Passive Circuit Design on Silicon

Spring 2024

The objective of this experiment is to explore circuit design, floor planning and layout using a simple passive circuit as an example. The design rules for this process can be found in this directory: /remote/cadencelib/tsmc018/PDK_doc/TSMC_DOC_WM/. The process parameters are summarized in the table appended to this document.

## Checkpoints

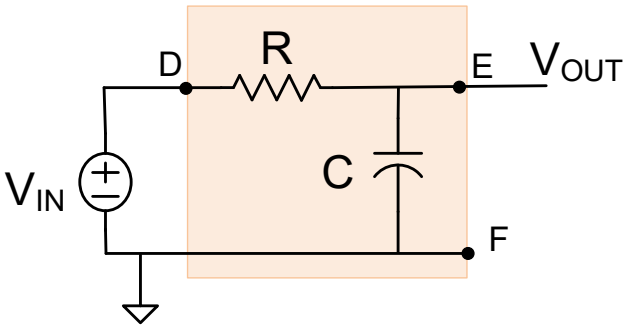
1. RC filter design.
2. Simulation of the RC filter showing the 3dB band edge.
3. Layout of the filter.
4. DRC/LVS check.

A first-order passive lowpass filter is shown below. The 3dB band edge, in rad/sec, of this circuit is given by the expression

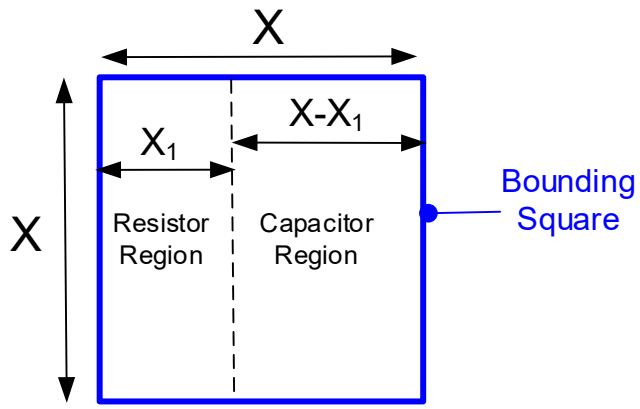
$$\omega_0 = \frac{1}{RC}$$

Design and layout this circuit using the TSMC 0.18µm CMOS process so that the 3dB band edge is 16MHz. The layout of this design should be embedded in a square and the design should have a goal of minimizing the total area of a bounding square. The bounding square is shown below. In this layout place the resistor in a rectangular region on the left side of the square and the capacitor in the rectangular region on the right side of the square. How you partition the area between the resistor and the capacitor, i.e. how $X_1$ is selected, is up to you. In this design, ground should be connected to the p-substrate. The 3 terminals denoted as D,E,and F should terminate in Metal 1. Use Poly to make the resistor. You may use any layers available in this process, except diffusions, to make the capacitor. When creating the resistor, assume any parasitic capacitances associated with the layout of the resistor can be neglected. Also neglect all fringe capacitances. The layout should satisfy all design rules for the process.

Hints: Remember, λ=0.3µm for this process. After determining what values are needed for R and C, do a floor plan so that you know where you will place your components. Give some thought to how you can use the layout editor efficiently to minimize the time required for the layout.




**First-order Lowpass Filter**




**Template for Layout**

| Passive Process Parameters for ON 0.5µm CMOS Process | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | N+ | P+ | POLY | POLY2 | HR_P2 | M1 | M2 | M3 | N/PLY | N_W | UNITS |
| RESISTANCES | | | | | | | | | | | |
| Sheet Resistance | 84 | 105 | 23.5 | 999 | 44 | 0.09 | 0.10 | 0.05 | 825 | 815 | Ohms/sq |
| Contact Resistance | 65 | 150 | 17 | | 29 | | 0.97 | 0.79 | | | Ohms |
| | | | | | | | | | | | |
| CAPACITANCES | | | | | | | | | | | |
| Area (substrate) | 425 | 731 | 84 | | | 27 | 12 | 7 | | 37 | af/µm$^2$ |
| Area (N+ active) | | | 2434 | | | 35 | 16 | 11 | | | af/µm$^2$ |
| Area (P+active) | | | 2335 | | | | | | | | af/µm$^2$ |
| Area (POLY) | | | | 938 | | 56 | 15 | 9 | | | af/µm$^2$ |
| Area (POLY2) | | | | | | 49 | | | | | af/µm$^2$ |
| Area (metal 1) | | | | | | | 31 | 13 | | | af/µm$^2$ |
| Area (metal 2) | | | | | | | | 35 | | | af/µm$^2$ |
| Fringe (substrate) | 344 | 238 | | | | 49 | 33 | 23 | | | af/µm |
| Fringe (poly) | | | | | | 59 | 38 | 28 | | | af/µm |
| Fringe (metal 1) | | | | | | | 51 | 34 | | | af/µm |
| Fringe (metal 2) | | | | | | | | 52 | | | af/µm |
| Overlap (N+active) | | | 232 | | | | | | | | af/µm |
| Overlap (P+active) | | | 312 | | | | | | | | af/µm |